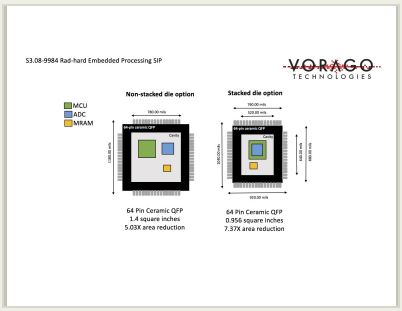
Small Business Innovation Research/Small Business Tech Transfer

Rad-Hard Embedded Processing SIP, Phase I

Completed Technology Project (2017 - 2017)

Project Introduction

VORAGO Technologies will create a design for a radiation-hardened miniaturized System-In-Package (SIP) that will comprise of an ARM-Cortex based microcontroller, an MRAM memory chip and an Analog-to-digital converter. The significance of the innovation is to enable a highly integrated SIP assembly that integrates multiple die from different processes and foundries, enabling a miniaturized, highly-reliable embedded processing / sensor interface module. The SIP will be optimized for size, weight, power consumption and radiation hardness. Based upon preliminary calculations, we expect that the SIP will be a minimum of 5X the area of implementing discrete chips. Combining multiple functions together will significantly reduce the mass and volume compared to existing solutions that would require at least three separate ICs to provide the same level of functionality. Designers will be able to reduce their PCB size and the amount of effort that it takes to layout and route a board. Fewer PCB connections and solder joints will improve the reliability of a design. A single SIP can also be tested and qualified more expediently than three individual devices. The technical objectives for the SIP are to select best-in-class radiation hardened semiconductor devices that offer a high level of performance, interoperability, very low power consumption and produce a design to integrate them into a single package. The resulting package footprint will be the smallest possible but will be designed so that it can be tested and qualified to MIL-PRF-38534. There are two package configurations that are possible to implement. One option does not involve die stacking and will reduce the area (versus using three standalone chips) of 5.03X. Another option uses a stacked die configuration and will result in an area reduction of 7.37X. After analyzing out both options in more detail, we will decide which option to pursue. A test and qualification plan will be provided.



Rad-hard Embedded Processing SIP, Phase I Briefing Chart Image

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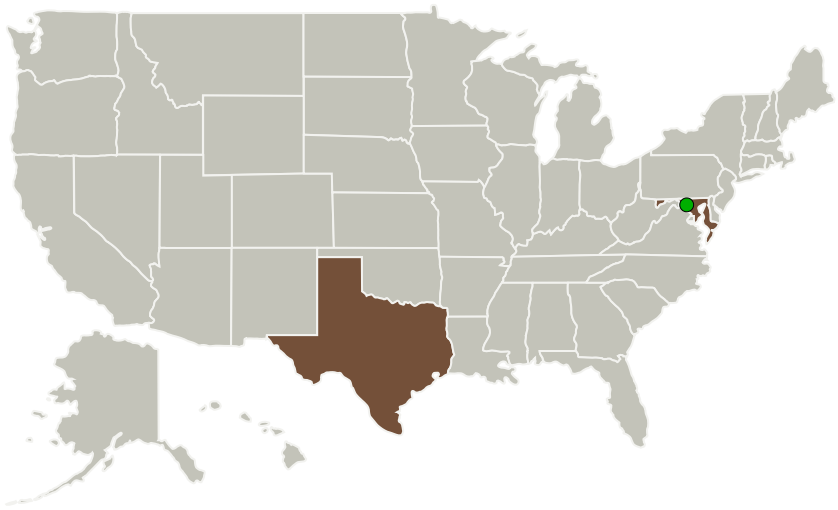
Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
Silicon Space Technology Corporation	Lead Organization	Industry	Austin, Texas
Goddard Space Flight Center(GSFC)	Supporting Organization	NASA Center	Greenbelt, Maryland

Primary U.S. Work Locations	
Maryland	Texas

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

Silicon Space Technology Corporation

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

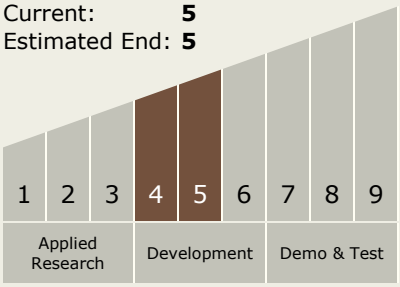
Carlos Torrez

Principal Investigator:

Ross Bannatyne

Technology Maturity (TRL)

Start: **4**
Current: **5**
Estimated End: **5**



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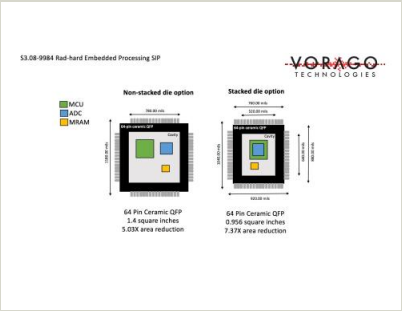
Images



Briefing Chart Image
Rad-hard Embedded Processing SIP, Phase I Briefing Chart Image *(https://techport.nasa.gov/image/126785)*

Technology Areas

Primary:

- TX02 Flight Computing and Avionics
  - TX02.1 Avionics Component Technologies
    - TX02.1.2 Electronic Packaging and Implementations